In re Patent Application of:
ROCHE ET AL.
Serial No. **10/039,765**
Confirmation No. **9186**
Filed: **NOVEMBER 7, 2001**
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In the Claims:

Claims 1-19 (Cancelled).

20. (Currently Amended) A method of transmitting data
between a master device and a slave device via a clock line and
at least one data line, the clock line being maintained by
default on a first logic value, and each master and slave device
being able to tie the clock line to a potential representing a
second logic value opposite the first logic value, the method
comprising:

when the master device is sending data to the slave
device and the slave device is receiving the data from the
master device, then

the master device applies data to the data
line, then ties the clock line to the second logic
value,

the slave device detects the second logic
value on the clock line, then ties the clock line to
the second logic value and reads the data,

the slave device maintains the tie to the
clock line at the second logic value while the slave
device has not read the data,

the slave releases the tie to the clock line
at the second logic value when the slave device has
read the data, and

the master device maintains the data on

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       the data line at least until an instant when the clock
line is released by the slave device,

           the master device releases the data on the
data line after the clock line is released by the
slave device and by the master device; and
when the slave device is sending data to the master
device and the master device is receiving the data from the
slave device, then

           the master device ties the clock line to the
second logic value,

           the slave device detects the second logic
value on the clock line, then ties the clock line to
the second logic value, and then or simultaneously
applies the data to the data line,

           the master device maintains the tie to the
clock line at the second logic value while the master
device has not read the data,

           the master device <u>releases</u> ~~release~~ the tie
to the clock line at the second logic value when the
master device has read the data,

           the slave device maintains the data on the
data line at least until an instant when the clock
line is released by the master device, and

           the slave device releases the data on the
data line after the clock line is released by the
master device and the slave ~~device~~ <u>device</u>, and

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        with the slave device tying the clock line

    to the second logic value every time the master device

    has tied the clock line to the second logic value,

    regardless of the direction in which the data is

    transmitted.

    Claims 21-23 (Cancelled).

    24. (Previously Presented) A method according to Claim
20, wherein a time period that the slave device has to release
the clock line after receiving data, is independent of any
action by the master device, as the master device does not send
any new data while the slave device has not released the clock
line.

    Claims 25-27 (Cancelled).

    28. (Previously Presented) A method according to Claim
20, wherein when the clock line has the first logic value, a
time period that the master device has to tie the clock line to
the second logic value is independent of any action by the slave
device.

    Claims 29-30 (Cancelled).

    31. (Previously Presented) A method according to Claim

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20, wherein the first logic value is 1 and the second logic value is 0.

        Claims 32-47 (Cancelled).

        48. (Currently Amended) A synchronous data transmission system comprising:
        a clock line;
        a data line;
        a master device comprising
                a clock line connection terminal connected to the clock line,
                at least one data line connection terminal connected to the data line,
                a circuit for tying the clock line to a potential representing a second logic value that is the opposite of a first logic value, and
                a data sending unit for waiting for the clock line to have the first logic value, applying data to the data line, tying the clock line to the second logic value after the data is applied to the data line, then releasing the clock line, and maintaining the data on the data line at least until the clock line has the first logic value, when the data is to be sent; and
        a slave device comprising

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a clock line connection terminal connected to the clock line,

at least one data line connection terminal connected to the data line,

a circuit for tying the clock line to the potential representing the second logic value,

a detector for detecting a change from the first logic value to the second logic value on the clock line, tying the clock line to the second logic value, reading the data on the data line, and releasing the clock line, when the data is to be received; and

wherein when said master device is sending data to said slave device and said slave device is receiving the data from said master device, then

said master device applies data to the data line, then ties the clock line to the second logic value,

said slave device detects the second logic value on the clock line, then ties the clock line to the second logic value and reads the data,

said slave device maintains the tie to the clock line at the second logic value while said slave device has not read the data,

said slave releases the tie to the clock line at the second logic value when said slave device

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has read the data, and

said master device maintains the data on the data line at least until an instant when the clock line is released by said slave device,

said master device releases the data on the data line after the clock line is released by said slave device and by said master device; and

wherein when said slave device is sending data to said master device and said master device is receiving the data from said slave device, then

said master device ties the clock line to the second logic value,

said slave device detects the second logic value on the clock line, then ties the clock line to the second logic value, and then or simultaneously applies the data to the data line,

said master device maintains the tie to the clock line at the second logic value while said master device has not read the data,

said master device releases ~~release~~ the tie to the clock line at the second logic value when said master device has read the data,

said slave device maintains the data on the data line at least until an instant when the clock line is released by said master device, and

said slave device releases the data on the

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data line after the clock line is released by said
master device and said slave device ~~device~~ device,
    with said slave device tying the clock line
to the second logic value every time said master
device has tied the clock line to the second logic
value, regardless of the direction in which the data
is transmitted.

49. (Previously Presented) A system according to Claim
48, wherein said master device further comprises a data
receiving unit for waiting for the clock line to have the first
logic value.

50. (Previously Presented) A system according to Claim
48, wherein said slave device further comprises a detector for
detecting a change from the first logic value to the second
logic value on the clock line.

Claims 51-52 (Cancelled).

53.   (New) A method according to Claim 21, further
comprising providing the slave device with a communication
interface circuit including:
    a trigger for automatically tying the clock line to the
second logic value when the clock line is changing from the
first logic value to the second logic value;

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an input for applying a clock line release signal to the trigger; and

an output for delivering a status signal that has a first value when the clock line is tied to the second logic value by the trigger and a second value when the clock line is released by the trigger.

54.   (New) A method according to Claim 53, wherein the communication interface circuit further comprises:

storage for storing at least one data; and

an applicator for automatically applying the at least one stored data to the data line when the clock line changes from the first logic value to the second logic value.

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